

CLAIMS

1. A programmable device comprising:
means for storing programmable information; and
means for providing a plurality of output clocks in
response to a reference clock frequency.

Sub a1 } 2. The circuit according to claim 1 wherein said
plurality of output clocks are individually programmable to a
plurality of frequencies.

3. The circuit according to claim 2 wherein said means
for providing said plurality of output clocks comprises a phase
lock loop (PLL).

4. The circuit according to claim 1 wherein said output
clock is accessible through one or more input/output pins.

5. The circuit according to claim 1 wherein said output
clocks have a particular impedance that may be adjusted to match
the impedance of an external device.

6. The circuit according to claim 1 wherein said output
frequencies can be programmed after fabrication and installation.

7. The circuit according to claim 1 wherein said reference clock frequency comprises one or more clock frequencies.

8. The circuit according to claim 7 wherein said inputs to said multiplexer are derived from one or more internally generated clocks.

9. The circuit according to claim 7 wherein said inputs to said multiplexer are derived from one or more externally generated clocks.

10. A device selected from the group consisting of programmable logic devices (PLDs), complex programmable logic devices (CPLDs) and field programmable gate arrays (FPGAs), comprising the circuit of claim 1.

11. The circuit according to claim 1 wherein an input delay and an output delay are reduced to zero.

12. A programmable device comprising:

a first circuit capable of storing programmable information; and

5 a second circuit capable of providing a plurality of output clock in response to a reference clock frequency, said second circuit comprising a phase locked loop (PLL).

Subar 13. The circuit according to claim 12 wherein said plurality of output clock are individually programmable to a plurality of frequencies.

14. The circuit according to claim 13 wherein said clocks have a particular impedance that may adjusted to match the impedance of an external device.

15. A method for providing an integrated programmable device and clock generation circuit comprising:

storing programmable information; and

5 generating a plurality of output clocks using a phase lock loop (PLL) in response to a reference clock frequency.

16. A method according to claim 16 comprising:
generating a plurality of output clocks that are
individually programmable to a plurality of independent
frequencies.

Subai } 17. A method according to claim 16 further comprising
adjusting the impedance to match the impedance of an external
device.

18. A method according to claim 16 further comprising:
generating said reference clock frequency in response to
one or more internally generated clocks.

19. A method according to claim 16 further comprising:
generating said reference clock frequency in response to
one or more externally generated clocks.

20. A method according to claim 16 further comprising:
generating said reference clock frequency in response to
one or more internally and externally generated clocks.

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